Listing of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously presented) A power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal functions as an input terminal of said power-up bias circuit, wherein said input terminal of said power-on bias circuit is further in electrical communication with a core voltage input terminal;

a second inverter having an input terminal and an output terminal, said output terminal of said second inverter functions as the output terminal for said power-up bias circuit; and

a Schmitt Trigger circuit having an input terminal and an output terminal, wherein said input terminal of the Schmitt Trigger circuit is connected to said output terminal of said first inverter, said output terminal of said Schmitt Trigger circuit is connected to said input terminal of said second inverter, said first inverter, said second inverter and said Schmitt Trigger circuit are each in electrical communication with a voltage input terminal and ground, wherein said voltage input terminal is an input/output voltage input terminal.

2. – 3. (canceled)

4. (previously presented) A power-on bias circuit according to claim 1, wherein said first inverter comprises a transistor of a first conductivity and a transistor of a second conductivity, a substrate and a source region of said transistor with the first conductivity are in electrical communication with said input terminal of said input/output terminal, a source and a substrate region of said transistor having the second conductivity is electrically connected to ground, a gate of said transistor with the first conductivity and the gate of said transistor with the second conductivity are electrically connected to said input terminal of said first inverter, a drain region of said transistor with the first conductivity and a drain region of said transistor with the second conductivity are electrically connected to said output terminal of said first inverter.

5. (Original) A power-on bias circuit according to claim 4, wherein said transistor of the first conductivity is a P-type transistor, said transistor of the second conductivity is an N-type transistor.

6. (previously presented) A power-on bias circuit according to claim 1, wherein said second inverter comprises a transistor of a first conductivity and a transistor of a second conductivity, a substrate and a source region of said transistor having the first conductivity are electrically connected to said input terminal of the input/output terminal, a source region of said transistor having the second conductivity is electrically connected to ground, a gate of said transistor having the first conductivity and the gate of said transistor having the second conductivity are electrically connected to said input terminal of said second inverter, a drain region of said transistor having the first conductivity and a drain region of said transistor having the second conductivity are electrically connected to said output terminal of said second inverter.

7. (Original) A power-on bias circuit according to claim 6, wherein said transistor having the first conductivity is a P-type transistor, said transistor having the second conductivity is an N-type transistor.

8. – 17. (canceled)

18. (previously presented) A power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal functions as an input terminal of said power-up bias circuit, wherein said input terminal of said power-on bias circuit is further in electrical communication with a core voltage input terminal;

a second inverter having an input terminal and an output terminal, said output terminal of said second inverter functions as the output terminal for said power-up bias circuit; and

a Schmitt Trigger circuit having an input terminal and an output terminal, wherein said input terminal of the Schmitt Trigger circuit is connected to said output terminal of said first inverter, said output terminal of said Schmitt Trigger circuit is connected to said input terminal of

said second inverter, said first inverter, said second inverter and said Schmitt Trigger circuit are each in electrical communication with a voltage input terminal and ground.